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Method Of Forming A Non-Volatile Resistance Variable Device, And Non-Volatile Resistance Variable Device

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Method Of F rming A Non-Volatile Resistance Variable Device, And Non-Volatile Resistance Variable Device

TECHNICAL FIELD

This invention relates to non-volatile resistance variable devices and methods of forming the same.

BACKGROUND OF THE INVENTION

Semiconductor fabrication continues to strive to make individual electronic components smaller and smaller, resulting in ever denser integrated circuitry. One type of integrated circuitry comprises memory circuitry where information is stored in the form of binary data. The circuitry can be fabricated such that the data is volatile or non-volatile. Volatile storing memory devices result in loss of data when power is interrupted. Non-volatile memory circuitry retains the stored data even when power is interrupted.

This invention was principally motivated in making improvements to the design and operation of memory circuitry disclosed in the Kozicki et al. U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796, which ultimately resulted from U.S. Patent Application Serial No. 08/652,706, filed on May 30, 1996, disclosing what is referred to as a programmable metalization cell. Such a cell includes opposing electrodes having an insulating dielectric material received therebetween. Received within the dielectric material is a fast ion conductor material. The resistance of such material can be changed

between highly insulative and highly conductive states. In its normal high resistive state, to perform a write operation, a voltage potential is applied to a certain one of the electrodes, with the other of the electrode being held at zero voltage or ground. The electrode having the voltage applied thereto functions as an anode, while the electrode held at zero or ground functions as a cathode. The nature of the fast ion conductor material is such that it undergoes a chemical and structural change at a certain applied voltage. Specifically, at some suitable threshold voltage, plating of metal from metal ions within the material begins to occur on the cathode and grows or progresses through the fast ion conductor toward the other anode electrode. With such voltage continued to be applied, the process continues until a single conductive dendrite or filament extends between the electrodes, effectively interconnecting the top and bottom electrodes to electrically short them together.

Once this occurs, dendrite growth stops, and is retained when the voltage potentials are removed. Such can effectively result in the resistance of the mass of fast ion conductor material between electrodes dropping by a factor of 1,000. Such material can be returned to its highly resistive state by reversing the voltage potential between the anode and cathode, whereby the filament disappears. Again, the highly resistive state is maintained once the reverse voltage potentials are removed. Accordingly, such a device can, for example, function as a programmable memory cell of memory circuitry.

The preferred resistance variable material received between the electrodes typically and preferably comprises a chalcogenide material having metal ions

diffused therein. A specific example is germanium selenide with silver ions. The present method of providing the silver ions within the germanium selenide material is to initially deposit the germanium selenide glass without any silver being received therein. A thin layer of silver is thereafter deposited upon the glass, for example by physical vapor deposition or other technique. An exemplary thickness is 200 Angstroms or less. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 500 nanometers. The thin nature of the deposited silver enables such energy to pass through the silver to the silver/glass interface effective to break a chalcogenide bond of the chalcogenide material, thereby effecting dissolution of silver into the germanium selenide glass. The applied energy and overlying silver result in the silver migrating into the glass layer such that a homogenous distribution of silver throughout the layer is ultimately achieved.

It can be challenging to etch and to chemical-mechanical polish metal ion containing chalcogenide materials. Accordingly it would be desirable to develop memory cell fabrication methods which avoid one or both of etching or polishing such materials. It would also be desirable to develop alternate methods from that just described which incorporate the metal ions into chalcogenide materials. While the invention was principally motivated in achieving objectives such as these, the invention is in no way so limited. The artisan will appreciate applicability of the invention in other aspects of processing involving chalcogenide materials, with the invention only being limited by the accompanying claims as literally worded and as appropriately interpreted in accordance with the doctrine of equivalents.

SUMMARY

The invention includes non-volatile resistance variable devices and methods of forming the same. In one implementation, a method of metal doping a chalcogenide material includes forming a metal over a substrate. A chalcogenide material is formed on the metal. Irradiating is conducted through the chalcogenide material to the metal effective to break a chalcogenide bond of the chalcogenide material at an interface of the metal and chalcogenide material and diffuse at least some of the metal outwardly into the chalcogenide material. In one implementation, a method of metal doping a chalcogenide material includes surrounding exposed outer surfaces of a projecting metal mass with chalcogenide material. Irradiating is conducted through the chalcogenide material to the projecting metal mass effective to break a chalcogenide bond of the chalcogenide material at an interface of the projecting metal mass outer surfaces and diffuse at least some of the projecting metal mass outwardly into the chalcogenide material. In certain aspects, the above implementations are incorporated in methods of forming non-volatile resistance variable devices.

In one implementation, a non-volatile resistance variable device in a highest resistance state for a given ambient temperature and pressure includes a resistance variable chalcogenide material having metal ions diffused therein. Opposing first and second electrodes are received operatively proximate the resistance variable chalcogenide material. At least one of the electrodes has a conductive projection extending into the resistance variable chalcogenide material.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at an alternate processing step subsequent to that shown by Fig. 3.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment 10 is shown in but one preferred embodiment of a method of forming a non-volatile resistance variable device. By way of example only, example such devices include programmable metalization cells and programmable optical elements of the patents referred to above, further by way of example only, including programmable capacitance elements, programmable resistance elements, programmable antifuses of integrated circuitry and programmable memory cells of memory circuitry. The above patents are herein incorporated by reference. The invention contemplates the fabrication techniques and structure of any existing non-volatile resistance variable device, as well as yet-to-be developed such devices. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the term "layer" encompasses both the singular and the plural unless otherwise indicated. Further, it will be appreciated by the artisan that

"resistance setable semiconductive material" and "resistance variable device" includes materials and devices wherein a property or properties in addition to resistance is/are also varied. For example, and by way of example only, the material's capacitance and/or inductance might also be changed in addition to resistance.

Semiconductor wafer fragment 10 comprises a bulk monocrystalline semiconductive material 12, for example silicon, having an insulative dielectric layer 14, for example silicon dioxide, formed thereover. A conductive electrode material 16, also termed a first metal layer, is formed over and on dielectric layer 14. By way of example only, preferred materials include any of those described in the incorporated Kozicki et al. patents referred to above in conjunction with the preferred type of device being fabricated. Layer 16 might constitute a patterned electrode for the preferred non-volatile resistance variable device being fabricated. Alternately by way of example only, layer 16 might constitute a patterned line or extension of a field effect transistor gate, with a subsequently deposited layer principally serving essentially as the electrode. An example preferred material for layer 16 is elemental tungsten deposited to an exemplary thickness of from about 100 Angstroms to about 1000 Angstroms. In the illustrated example, layer 16 has been patterned, and another dielectric layer 17 has been deposited and planarized as shown.

A second metal layer 18 is formed (preferably by a blanket deposition) on first metal layer 16. An exemplary preferred material in conjunction with the non-volatile resistance variable device being fabricated is elemental silver.

A preferred thickness for layer 18 is from about 175 Angstroms to about 300 Angstroms.

Referring to Fig. 2, second metal layer 18 is formed into a structure 20, and first metal layer 16 is outwardly exposed. Such is preferably conducted by subtractive patterning of metal layer 18, for example by photolithographic patterning and etch. In one implementation, structure 20 can be considered as comprising a metal mass projecting from underlying substrate material and having outer surfaces comprised of a top surface 22 and opposing side surfaces 24 which join with top surface 22 at respective angles. The preferred angles are preferably within about 15° of normal, with normal angles being shown in the figures.

Referring to Fig. 3, a chalcogenide material 26 is formed over the substrate on second metal structure 20 outer surfaces 22 and 24, and on exposed first metal layer 16. Such is preferably formed by blanket physical vapor deposition. A preferred deposition thickness for layer 26 is preferably less than three times the thickness of deposited layer 18, with an example being from about 525 Angstroms to about 900 Angstroms. More preferred is a thickness to provide layer 18 at 20% to 50% of layer 26 thickness. Exemplary preferred chalcogenide materials include those disclosed in the Kozicki et al. patents referred to above. Specific preferred examples include a chalcogenide material having metal ions diffused therein represented by the formula Ge_xA_y, where "A" is selected from the group consisting of Se, Te and S and mixtures thereof. The illustrated example provides but one possible example of surrounding the exposed outer surfaces of a projecting

metal mass with chalcogenide material in accordance with but one aspect of the invention.

Referring to Fig. 4, irradiating is conducted through chalcogenide material 26 to patterned second metal 18 effective to break a chalcogenide bond of the chalcogenide material at an interface with the patterned second metal outer surfaces and the chalcogenide material, and to diffuse at least some of second metal 18 outwardly into the chalcogenide material. Metal doped material 27 is formed thereby. Therefore as shown in the preferred embodiment, only a portion of blanket deposited chalcogenide material layer 26 is doped with second metal 18. A preferred irradiating includes exposure to actinic radiation having a wavelength below 500 nanometers, with radiation exposure at between 404 - 408 nanometers being a more specific example. A specific example in a suitable UV radiation flood exposure tool is 4.5 mW/cm^2, 15 minutes, 405 nm wavelength, at room ambient temperature and pressure.

In the depicted and preferred embodiment, the irradiating diffuses only some of the metal from layer 18 outwardly into chalcogenide material, leaving a remnant structure 20a. Accordingly, the projecting metal mass 20a has a shape after the irradiating which is maintained in comparison to original shape 20, but at a reduced size. Fig. 5 illustrates a lesser preferred alternate embodiment 10a whereby the irradiating and/or layer dimensions might be modified such that the irradiating diffuses all of projecting metal mass 20 outwardly into the chalcogenide material.

The preferred exemplary tungsten material of layer 16 does not appreciably diffuse into layer 26. Referring to Fig. 6 and regardless, chalcogenide material 26 not doped with metal 18 is substantially selectively etched from metal doped portion 27 of the chalcogenide material. In the context of this document, "substantially selective" means a relative etch ratio of layer 26 relative to layer 27 or at least 3:1. In the illustrated and preferred embodiment, such etching is preferably conducted to remove all of chalcogenide material 26 which has not been doped with metal 18. The preferred etching comprises dry anisotropic etching, preferably dry plasma anisotropic etching. A principle preferred component of such etching gas comprises CF_4. Additional preferred gases in the chemistry include C_2F_6 and C_4F_8. Top power is preferably maintained at 500 watts, with the lower wafer susceptor being allowed to float. Susceptor temperature is preferably maintained at about 25°C, and an exemplary reactor pressure is 50 mTorr. By way of example only, a specific example in a reactive ion etcher is CF_4 at 50 sccm, Ar at 25 sccm, susceptor temperature at 25°C, pressure of 50 mTorr and top power at 500 Watts.

Referring to Fig. 7, an insulating layer 30 has been deposited and metal doped chalcogenide material 27 has been exposed. An example and preferred material for layer 30 is silicon nitride.

Referring to Fig. 8, an outer conductive electrode layer 32 has been deposited and patterned to form the outer electrode of the preferred non-volatile resistance variable device. Example materials include those disclosed in the above Kozicki et al. patents. In the illustrated and described preferred

example, silver structure 20a might be designed and fabricated to constitute the effective quantity of silver for programming the device with no silver being provided in electrode 32. Alternately by way of example only, layer 16 might also constitute elemental silver with no silver being provided in electrode 32. Further, by way of example only, electrode 32 might principally comprise elemental silver, or at least a lower silver portion in contact with the chalcogenide material 27.

The above-described preferred embodiment example was in conjunction with fabrication of a non-volatile resistance variable device. However, the invention also contemplates metal doping a chalcogenide material independent of the device being fabricated, and in the context of the accompanying claims as literally worded regarding methods of metal doping a chalcogenide material. Further, the preferred example is with respect to formation of a projecting metal from an underlying substrate having chalcogenide material received thereover. However, the invention is in no way so limited and also contemplates, by way of example only, diffusing metal from an entirely flat, or other, underlying surface into overlying chalcogenide material.

The invention also contemplates non-volatile resistance variable devices independent of the method of manufacture. In one implementation, such a device includes a projecting metal mass (for example mass 20a) extending outwardly from a first metal layer laterally central into resistance variable chalcogenide material. In one aspect, the invention contemplates the device being in a highest resistance state for a given ambient temperature and pressure. For example, the Fig. 8 device as depicted is in such a highest

state of resistance. Progressively lower states of resistance for a given ambient temperature and pressure will exist as a silver dendrite, in the preferred embodiment, progressively grows from an electrode to the point of contacting the opposing electrode. Fig. 8 depicts but one exemplary embodiment of such a non-volatile resistance variable device having such a laterally central located projecting mass relative to material 27.

The invention also contemplates a non-volatile resistance variable device in a highest resistance state for a given ambient temperature and pressure independent of a conductive projection which is so centrally located. Such comprises a resistance variable chalcogenide material having metal ions diffused therein. Opposing first and second electrodes are received operatively proximate the resistance variable chalcogenide material, with at least one of the electrodes comprising a conductive projection extending into the resistance variable chalcogenide material. Provision of such a structure is in no way shown or suggested in a highest resistance state for a given ambient temperature and pressure in any of the teachings and drawings of the above-described Kozicki et al. patents.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper

scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.